63.2% High Efficiency and High Linearity Two-stage InGaP/GaAs HBT Power Amplifier for Personal Digital Cellular Phone System

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ABSTRACT

This paper reports on a high efficiency and high linearity two-stage InGaP/GaAs heterojunction bipolar transistor (HBT) power amplifier for the Japanese personal digital cellular phone system (PDC). Our power-stage HBT amplifier exhibited a high power added efficiency (PAE) of 68.8% and an adjacent channel leakage power (ACP) of -48 dBc. The ACP of the two-stage amplifier was improved enough for PDC with keeping a high PAE by combining of a driver-stage and this power-stage amplifiers. Our two-stage HBT power amplifier exhibited the highest PAE of 63.2% ever reported and an ACP at a 50-kHz offset frequency of -52 dBc in 1.5 GHz PDC standard at a Pout of 31 dBm under a supply voltage of 3.5 V.

1. INTRODUCTION

Current digital mobile communication systems require high efficiency, high linearity, and low cost power amplifier for handset transmitters. HBTs are the one of the most promising devices due to their high efficiency and high linearity [1-4], and their higher power handling capability with a small chip size [5].

In handset transmitters, two- or three-stage power amplifier modules are usually used. There are several papers which discussed linearity and power characteristics of power amplifiers, such as a trade-off between efficiency and linearity in conjunction with operating class [6], or input and output terminations [7]. The discussion is, however, restricted to the power-stage amplifier only.

In this work, the effect of the phase distortion on ACP is analyzed to improve both efficiency and linearity. Phenomenon of the ACP improvement in the two-stage amplifier is discussed in comparison with the experimental results of the driver-stage and the power-stage amplifiers.

2. DEVICE FABRICATION

We fabricated InGaP/GaAs HBTs. InGaP/GaAs HBT has a high reliability at a high current density, which is desirable for decreasing a device size namely for low cost. It also has a smaller collector emitter offset voltage in comparison with AlGaAs/GaAs HBT, which is an advantage for low-bias voltage operation. The schematic cross-sectional view of InGaP/GaAs HBT is shown in Fig. 1. The InGaP/GaAs HBT structure grown by MOCVD consists of an n^+-InGaAs cap layer, an n-InGaP emitter layer, a C-doped p^+-GaAs base layer, an n/i-GaAs collector layer, and an n^+-GaAs sub-collector layer. The collector consists of a 200 nm n^--GaAs and 400 nm i-GaAs layer [8]. The HBT structure has a plated heat sink (PHS) with via holes. The fabricated driver-stage and power-stage HBT amplifiers have 8 fingers and 48 fingers of 2 x 20 μm emitter, respectively.

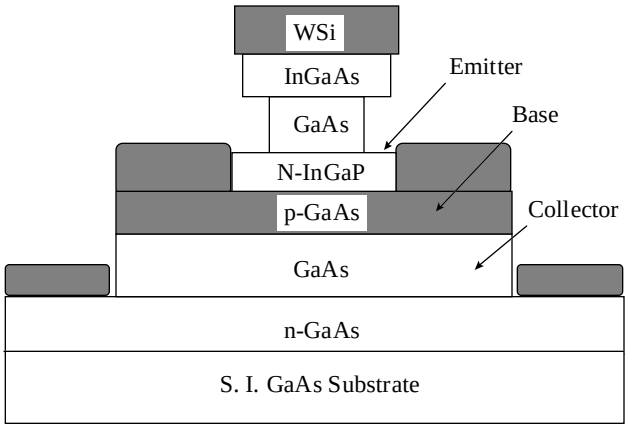

Fig. 1. Schematic cross-sectional view of InGaP/GaAs HBT.

3. DC AND SMALL SIGNAL CHARACTERISTICS

The DC and RF measurements were performed on one finger HBT with an emitter area of 2 x 20 μm. The collector emitter offset voltage ($V_{CE\text{-}offset}$) was 80 mV, which is 0.1- 0.3 V lower than that of the AlGaAs/GaAs HBT. The breakdown voltage at an open base (BV_{CEO})was 14 V, which is enough to an operation voltage of 3.5 V. The f_T and f_{max} of the InGaP/GaAs HBT with an emitter area of 2 x 20 • m were 40 and 110 GHz respectively, at a collector

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current (I_C) of 16 mA and a collector bias (V_{CE}) of 3.5 V. The MTTF of our HBTs is 1 x 10^6 hours at a collector current density of 6 x 10^4 A/cm^2 and a junction temperature (T_j) of 200°C [9] .

4. POWER PERFORMANCE OF POWER-STAGE AMPLIFIER

First, we performed a load-pull measurement for the power-stage amplifier at 1.5 GHz biased under class A-B. The supply voltage (V_{CE}) was 3.5 V and the quiescent collector current (I_{Cq}) was 100 mA. We used an ATN automatic load-pull measurement system (LP-1). In an ACP measurement, we used LP-1 with an Anritsu spectrum analyzer (MS2602A), and digital modulation signal generator (MG3670A), which generate a PDC 1.5 GHz π/4-shift QPSK modulated signal.

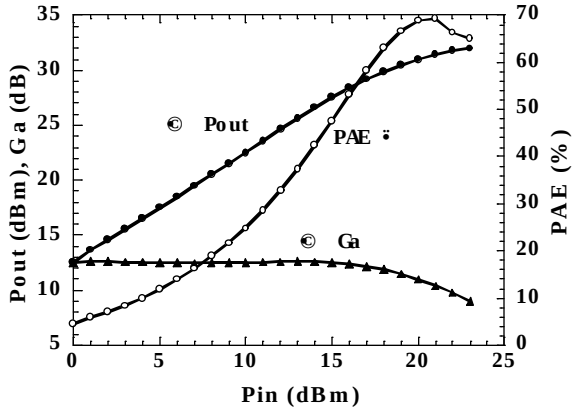

Fig. 2a. Pout, Gain (Ga), and PAE versus input power (Pin) of the power-stage amplifier.

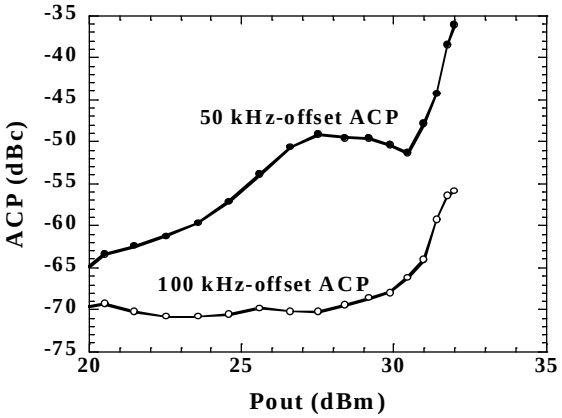

Fig. 2b. ACP versus Pout of the power-stage amplifier.

The power-stage amplifier characteristics are shown in Fig. 2a. and 2b., when the output matching circuit is optimized for high efficiency and moderate linearity.

Power gain compression and phase distortion are important behavior parameters to predict ACP. Fig. 3. shows our circuit simulation results of ACP. In the case with the phase distortion and the gain compression (case A), we simulated considering the phase distortion and the gain compression. In the case without the gain compression (case B), we simulated considering only the phase distortion. In the case without the phase distortion (case C), we simulated considering only the gain compression. The behavior of ACP in the case A at a Pin below 18 dBm agrees well with that in the case B. Therefore, the behavior of ACP at a lower Pout (or Pin) is dominated by the phase distortion. At a high Pout (Pin > 19 dBm), the ACP in the case C drastically increases, and in the case A, it also increases, but in the case B, it decreases. The behavior of ACP in a high Pout region (Pin > 19 dBm) is dominated by the gain compression.

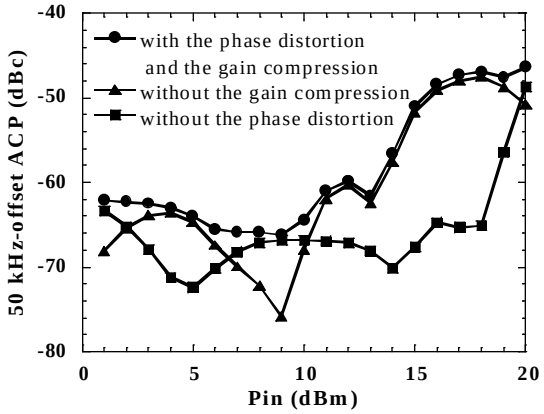

Fig. 3. Circuit simulation results of ACP
: the cause of the ACP degradation.

From the comparison with our simulation results, the ACP around a Pout of 31 dBm in Fig. 2b. is influenced by both the gain compression and the phase distortion. To reduce the ACP at a Pout of 31 dBm, we have to decrease the gain compression or the phase distortion. The decrease of the gain compression, however, causes the degradation of PAE. Therefore, we tried to decrease the phase distortion. The power-stage amplifier exhibited a high PAE of 68.8%, and an ACP of -48 dBc at a Pout of 31 dBm.

5. POWER PERFORMANCE OF TWO-STAGE AMPLIFIER

Next we performed a source-pull measurement for the two-stage amplifier at 1.5 GHz biased under class A-B. The supply voltage (V_{CE}) was 3.5 V and the I_{Cq} of the driver-stage amplifier and the power-stage amplifier were 20 mA and 100 mA, respectively. The load impedance was the same as when we measured the power characteristics of the power-stage amplifier to keep a high PAE. We connected the driver-stage to the power-stage via a DC-cut capacitor. Fig. 4. shows ACP at a 50 kHz-offset frequency of driver-stage, power-stage, and two-stage amplifiers as a function of Pout. When we measured the driver-stage power characteristics, the source impedance was the same as that of the two-stage measurement and the load impedance was tuned to the power-stage input impedance when the power-stage was operating at a Pout of 31 dBm. The Pout of the driver-stage is replaced by the Pout of the two-stage to compare behavior of several stages, easily.

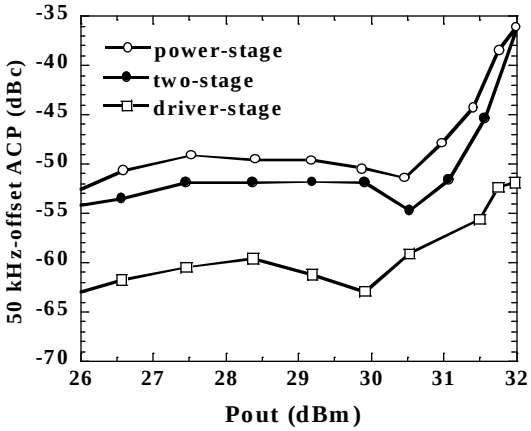

Fig. 4. 50 kHz-offset ACP versus Pout of driver-stage, power-stage, and two-stage amplifiers.

Despite a degradation of the ACP of the driver-stage amplifier at a Pout of 31 dBm, the ACP of two-stage amplifier is improved to -52 dBc compared with -48 dBc of the power-stage amplifier at a Pout of 31 dBm. We also performed AM-PM and AM-AM measurement of the driver-stage, the power-stage, and the two-stage amplifiers. The results of ACP, the phase distortion ($\Delta\phi$), and the gain compression (ΔGa) at a Pout of 31 dBm are summarized in Table 1.

	driver-stage	power-stage	two-stage
ACP	**- 49 dBc**	**- 48 dBc**	**- 52 dBc**
$\Delta\phi$	**-0.36 deg**	**- 1.42 deg**	**0.60 deg**
Δ Ga	**0.04 dB**	**1.52 dB**	**1.68 dB**

Table 1. Summary of ACP, phase distortion, and gain compression at a Pout of 31 dBm.

The results indicate three things. First, in comparison of the two-stage and the power-stage results, the reduction of $\Delta\phi$ is important to improve ACP, which agree with our simulation results. At a Pout of 31 dBm, the ACP of two-stage amplifier was improved by the reduction of $\Delta\phi$ with keeping a high PAE.

Second, $\Delta\phi$ of the two-stage is not equal to the sum of $\Delta\phi$ of the driver-stage and the power-stage. Both $\Delta\phi$ of the driver-stage and the power-stage have negative value, however, $\Delta\phi$ of the two-stage has a positive value. The phase compensation technique between the driver-stage and the power-stage is not simple as a theory. As the driver-stage measurement, the load was tuned to the input impedance of the power-stage. However, we could not measure the accurate input impedance of the power-stage in a large signal operation. The reason why the experimental results of $\Delta\phi$ behavior is different form a theory may be due to the inaccuracy of the load impedance when we measured the AM-PM of the driver-stage.

Third, the ACP of the two-stage is lower than that of the power-stage in a power range (Pout > 26 dBm). The peak power of the modulated signal is about 3 dB higher than its average power. The driver-stage amplifier may reduce the peak to average ratio due to its gain compression characteristics. This small ratio signal to the power-stage amplifier may result in a reduction of a spectrum regrowth in the output signal. Further consideration is needed.

Experimental results of the two-stage amplifier are shown in Fig. 5a. and 5b. We achieved a high PAE and high linearity simultaneously by the reduction of the total $\Delta\phi$. The 50 kHz-offset ACP for the • /4-shift QPSK signal of the two-stage power amplifier is finally improved to -52 dBc with a high PAE of 63.2% at a Pout of 31 dBm.

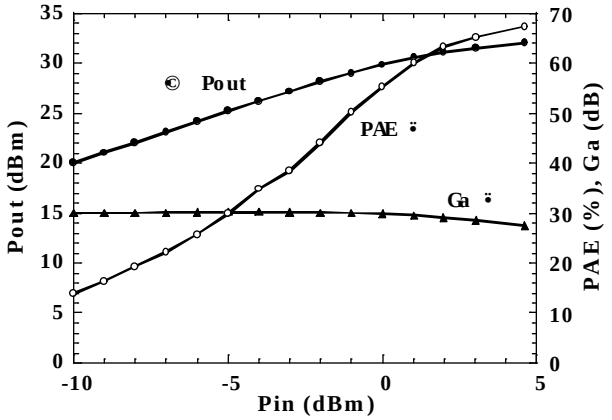

Fig. 5a. Pout, Ga, and PAE versus Pin of the two-stage amplifier.

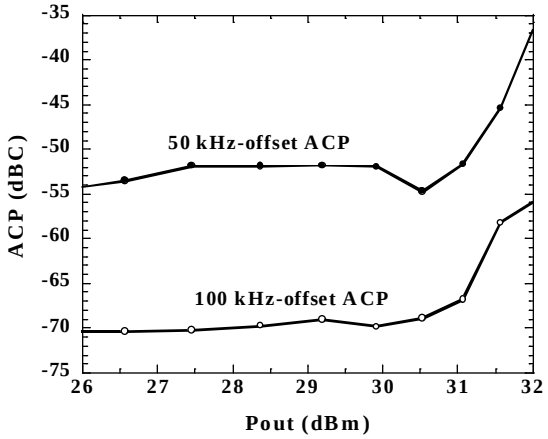

Fig. 5b. ACP versus Pout of the two-stage amplifier.

6. CONCLUSION

We presented the unexplored performance of InGaP/GaAs HBT two-stage power amplifier having a PAE of 63.2% and an ACP of -52 dBc in 1.5GHz PDC standard. We achieved a high PAE and a superior ACP simultaneously by minimizing the total phase distortion at a Pout of 31 dBm under a supply voltage of 3.5 V.

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REFERENCE

[1] R .S. Brozovich, D. R. Helms, L. W. Yang, and J. J. Komiak, "A Highly Linear Highly Efficient HBT for Communication Circuit," IEEE GaAs IC Symposium, pp.291-293, 1994.

[2] N. L. Wang, W. J. Ho, and J. A. Higgins, "AlGaAs/GaAs HBT Linearity Characteristics," IEEE Trans. Microwave Theory Tech., vol.42, pp.1845-1994, 1994.

[3] J. J. Komiak, and L. W. Yang, "Highly Linear Efficient HBT MMIC Power Amplifiers," IEEE GaAs IC Symposium, pp.295-298, 1994.

[4] P. Walters, P. Lau, K. Buehring, J. Penny, C. Farley, P. McDade, and K. Weller, "A Low Cost Linear AlGaAs/GaAs HBT MMIC Power Amplifier With Active Bias Sensing for PCS Application," IEEE GaAs IC Symposium, pp.67-70, 1995.

[5] Y. Tateno, H. Yamada, S. Ohara, S. Kato, H. Ohnishi, T. Fujii, and J. Fukaya, "3.5 V, 1 W High Efficiency AlGaAs/GaAs HBTs with Collector Launcher Structure," 1994 IEDM Tech. Dig., pp.195-198.

[6] C. Pinatel, S. Vuye, M. Riet, C. Dubon-Chevalier, B. Rojat, and A. Lermoyer, "Trade off analysis between power-added efficiency and linearity on HBT power amplifier," Proc. of 25th European Microwave Conference 1995, Vol. 1, pp. 20-23.

[7] H. Yamada, S. Ohara, T. Iwai, Y. Yamaguchi, K. Imanishi, and K. Joshin, "Self-Linearizing Technique for L-Band HBT Power Amplifier: Effect of Source Impedance on Phase Distortion," IEEE Trans. Microwave Theory and Tech., Vol. 44, No. 12, pp. 2398-2402, 1996.

[8] S. Ohara, H. Yamada, T. Iwai, Y. Yamaguchi, K. Imanishi, and K. Joshin, "InGaP/GaAs Power HBTs with a Low Bias Voltage," 1995 IEDM Tech. Dig., pp. 791-794.

[9] T. Takahashi, S. Sasa, A. Kawano, T. Iwai, and T. Fujii, "High-Reliability InGaP/GaAs HBTs Fabricated by Self-Aligned Process," 1994 IEDM Tech. Dig. , pp. 191-194.